MEMORY DEVICE WITH DATA LINE STEERING AND BITLINE REDUNDANCY

Abstract of the Disclosure

An integrated circuit including: a set of bitlines; a set of data lines; means for coupling each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, the second respective bitline being adjacent to the first respective bitline; and means for maintaining the first respective bitline at a desired potential after the data line is coupled to the second bitline.

Figures